Microstructures Comprising a Dielectric Layer and a Thin Conductive Layer

David W. Sherrer

Related Applications

[0001] This application is a continuation-in-part application of U.S. Application No. 09/541,394, filed March 31, 2000, the entire contents of which are incorporated herein by reference.

Field of the Invention

[0002] The present invention relates to micromachined structures. More specifically, the present invention relates to released, flexing, and/or suspended multilayer microstructures having a first layer of a structural dielectric material (e.g. silicon nitride) to provide structural support for the released/suspended layer and second layer of an electrically conductive material (e.g. doped polysilicon) disposed over the first layer.

Background of the Invention

[0003] Released microstructures are commonly used in a variety of sensors, actuators and other useful devices. Released microstructures are suspended above a substrate (e.g. silicon) to which they are usually attached or anchored. Examples of released microstructures include comb drives, cantilevers, beams, membranes, switches, electrostatic motors and a wide variety of sensors (e.g. pressure sensors, magnetic sensors).

[0004] Released microstructures are often made from polysilicon. This is because polysilicon can be conformally deposited on many surfaces and it can be doped to provide conductivity. Also, polysilicon is easily released because there are a number of supporting materials available that can be selectively etched from under or surrounding a polysilicon layer (e.g. phosphosilicate glass, PSG). However, polysilicon has the great disadvantage that deposited polysilicon layers can have relatively high internal stress. Therefore, polysilicon structures tend to distort and bend when released. The tendency of polysilicon to bend after release is undesirable for making precision micromachined structures. Another disadvantage of polysilicon is that it can have a relatively low

strength. In addition, polysilicon can have various states of crystallinity – ranging from relatively amorphous to having relatively large crystal grains. The size of these grains and their orientation effects the mechanical properties of the polysilicon layer. Even when polysilicon is deposited with the desired mechanical properties and grain size, the thermal budget in later processing may cause changes in these properties due to grain growth, precipitation at the grain boundaries, and other physical phenomena. For example, doped amorphous polysilicon may become significantly polysilicon during a LPCVD silicon nitride or PSG deposition that occurs after its deposition.

[0005] Polysilicon can be annealed to reduce internal stress and reduce bending. However, polysilicon annealing techniques are cumbersome and can interfere with other process steps required in making a useful device. It would be an improvement in the art to obviate polysilicon annealing in making certain released microstructures.

[0006] Due to these disadvantages of polysilicon, silicon nitride is sometimes used instead for released microstructures. Low stress silicon nitride films are readily formed without annealing by increasing the silicon content of the film. Also, silicon-rich silicon nitride is rigid, strong, and can be released from a variety of supporting layers. A problem with silicon nitride is that it is an electrical insulator, preventing the ability to charge and discharge the surface as is required in electrostatic actuators. Further, it can not be used alone to conduct a voltage or current as may be desired in electrical switching. For devices that require a thermally conductive released microstructure it may not be desirable or possible to use silicon nitride. Likewise, for devices in which high thermal conductivity is desirable, such as for heat dissipation, it may not be desirable or possible to use silicon nitride.

[0007] Therefore, there is a need in the art for an electrically conductive material that can form low internal stress, high strength micro structures. Such a material could be used in a wide variety of released microstructures. In addition, there is a need in certain applications for materials with high thermal conductivity.

[0008] US patent 5,936,159 to Kano et al. discloses a released cantilever having a three-layer structure. The middle layer is a very thin stress relieving layer that tends to equalize stress in the cantilever, thereby reducing bending. In a preferred embodiment,

a stress relieving layer tens of angstroms thick is disposed between thicker films of polysilicon.

[0009] US patent 5,475,318 to Marcus et al. discloses a micromachined cantilever probe for contacting integrated circuits. The cantilever has two layers with different coefficients of expansion. When heated, the cantilever bends to provide electrical contact with a nearby electrical pad.

[0010] US patent 5,866,805 to Han et al. discloses a cantilever having a magnetic thin film. The magnetic thin film provides magnetic coupling to a nearby electromagnet. The electromagnet can cause the cantilever to vibrate for use in 'AC mode' force microscopy. A second layer is applied to the cantilever to reduce bending of the cantilever.

[0011] US patent 5,796,152 to Carr et al. discloses a cantilever having two separately bendable actuator sections. Each section can be heated separately. In is way, the cantilever can be caused to bend in complex shapes such as S-curves.

Summary of the Invention

[0012] In a first aspect of the present invention, a micromachined apparatus is provided comprising a substrate and a released microstructure disposed on the substrate, the microstructure comprising a dielectric layer and a conductive polysilicon layer attached to the dielectric layer, wherein the polysilicon layer has a thickness less than 1/5 the dielectric layer thickness. In a second aspect of the present invention, a micromachined apparatus is provided comprising a substrate and a released microstructure disposed on the substrate, the microstructure comprising a dielectric layer and a conductive layer attached to the dielectric layer, wherein the conductive layer has a thickness less than 1/5 the dielectric layer thickness.

Brief Description of the Drawings

[0013] The foregoing summary and the following detailed description of the preferred embodiments of the present invention will be best understood when read in conjunction with the appended drawings, in which:

[0014] Fig. 1 shows a cantilever according to the present invention;

[0015] Fig. 2 shows an alternative embodiment having both top and bottom conductive layers;

[0016] Fig. 3 shows a cantilever and a conductive pad for electrostatic actuation of the cantilever;

[0017] Fig. 4 shows a cantilever with a conductive layer on the top surface;

[0018] Figs. 5a-e illustrate a preferred method for making the present invention;

[0019] Fig. 6 shows an alternative embodiment with a conductive layer disposed within the dielectric layer;

[0020] Fig. 7 shows an alternative embodiment of the present invention having vias for electrically connecting top and bottom conductive layers;

[0021] Fig. 8 shows a cross sectional view of a cantilever of the present invention having a conductive layer on the top surface and sidewalls;

[0022] Figs. 9a-9f illustrate a method for making the cantilever shown in Fig. 8;

[0023] Fig. 10 shows an embodiment of the present invention where the dielectric layer is enclosed with conductive polysilicon; and

[0024] Fig. 11 shows a particularly useful application of the present invention for a microelectrooptomechanical variable reflector.

Detailed Description of the Invention

[0025] The present invention provides released microstructures having a dielectric layer, such as silicon nitride or silicon carbide, combined with a much thinner layer (e.g., 1/5, 1/10, 1/50 or 1/100 the thickness of the dielectric layer) of a conductive material, such as a metal or polysilicon. The thin conductive layer can be located on the top side and/or bottom side of the dielectric layer, or within the dielectric layer. The relatively thick dielectric layer provides good mechanical properties for the microstructure (e.g., high strength, low internal stress, high rigidity). The conductive layer is sufficiently thin so that it does not adversely affect the mechanical properties of the microstructure. The thin conductive layer provides electrical conductivity so that the microstructure can be used in electrostatic actuators, piezoresistive devices and other microelectromechanical systems (MEMS), or micro-electro-opto-mechanical devices. Preferably, the conductive

layer is highly conductive (e.g., if polysilicon, heavily doped) so that it can be exceptionally thin (e.g., less than 25 nanometers) and still provide good surface conductivity. For example, the dielectric layer thickness may desirably be in the range of about 2-50 microns and the conductive layer thickness in the range of 5-50 nanometers. Alternatively, the dielectric layer thickness and conductive layer thickness may be 2-50 microns and 1-1000 nanometers, respectively, or 3-50 microns and 1-100 nanometers, respectively, or 5-50 microns and 5-50 nanometers, respectively, for example. Of course, the required conductivity and thickness of the conductive layer depend upon the microstructure design and its application.

[0026] Fig. 1 shows a simple cantilever 20 according to the present invention. The cantilever 20 is attached to a substrate 22 made of silicon or silica, for example (other substrates can also be used). The cantilever comprises a relatively thick dielectric layer 24, and a relatively thin conductive layer 26 on a bottom side of the cantilever. The dielectric layer 24 and the conductive layer 26 are bonded together, and both can be formed using low pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition. The conductive layer 26 is thin enough relative to the dielectric layer 24 such that the mechanical properties (e.g., strength, internal stress, rigidity) of the cantilever are primarily determined by the dielectric layer. The electrical conductivity of the cantilever is primarily determined by the conductive layer 26.

[0027] According to the present invention, the conductive layer 26 may desirably have a thickness less than 1/5 the thickness of the dielectric layer 24. Preferably, the conductive layer thickness is less than 1/10, 1/20, 1/30, 1/50, or 1/100 the dielectric layer thickness. Thin conductive layers are preferred, because they have a small effect on the mechanical properties of the cantilever or microstructure. In addition, materials for the dielectric layer may desirably be chosen which have a thermal conductivity of at least 50 Watts per meter Kelvin.

[0028] If polysilicon is used in the conductive layer 26, the polysilicon may preferably have a dopant concentration greater than about 10^{17} per cubic centimeter, more preferably, greater than 10^{18} or 10^{20} atoms per cubic centimeter. Polysilicon can be doped with phosphorous, boron, or any other dopant that imparts conductivity. Preferably, the polysilicon is doped with a material that can be incorporated during LPCVD or PECVD

deposition (e.g., phosphorous). The dopant level in polysilicon can have a wide range of values. The dopant level should be high enough to provide adequate surface conductivity necessary for the intended use of the microstructure (e.g., electrostatic actuation, piezoresistive sensing, switching or electrostatic charge dissipation). In many microelectromechanical applications, surface conductivity (Ohms per square) of the conductive layer is the important consideration.

[0029] Fig. 2 shows an alternative embodiment of the present invention where the cantilever 20 has a first conductive layer 26a and a second conductive layer 26b. The dielectric layer 24 is sandwiched between the conductive layers 26a, 26b. Each conductive layer has a thickness less than 1/5 the thickness of the dielectric layer. More preferably, each conductive layer is less than 1/10 or 1/20 the thickness of the dielectric layer. Preferably, the thicknesses of the conductive layers 26a, 26b are equal. The conductive layers 26a, 26b are thin enough so that the mechanical properties of the cantilever are primarily determined by the dielectric layer 24. A benefit of this structure is that the stresses in the conductive layer can counterbalance each other producing a near net zero stress effect on the structural layer to prevent deflection. Alternatively, the thickness of the layers can be made of two different thicknesses to impart a net stress force on the structural layer. This could be useful to establish a state of curl or static deflection in a cantilever.

[0030] Fig. 3 shows a cantilever device of the present invention in operation. A conductive pad 28 disposed on the substrate 22 is electrostatically coupled to the conductive layer 26. Applying a voltage between the conductive pad 28 and the conductive layer 26 causes the cantilever to move with respect to the substrate 22. The conductive layer 26 also assures that electrostatic charges in the dielectric layer 24 are rapidly dissipated. As noted, the mechanical properties of the cantilever are primarily determined by the dielectric layer 24.

[0031] Fig. 4 shows another embodiment of the present invention where the conductive layer 26 is disposed on top of the dielectric layer 24. The dielectric layer 24 may desirably comprise silicon rich (SiN) low stress dielectric. Other stoichiometries can also be used. Preferably, the internal stress in the dielectric layers is in the range of -300 to

+300 MPa. More preferably, the dielectric layer often has an internal tensile stress in the range of 20-300 MPa tensile stress.

[0032] Figs. 5a-5e illustrate a preferred method for making the microstructures of the present invention. First, in Fig. 5a, phosphosilicate glass (PSG) 30 is deposited and patterned on a substrate 22 (e.g., a silicon or quartz substrate). There are many well known processes for depositing and patterning PSG.

[0033] Next, in Fig. 5b, conductive material is deposited conformally on the PSG 30. Preferably, the conductive layer 32 is deposited by low-pressure chemical vapor deposition, and if polysilicon is used it may be doped as it is deposited. For example, the polysilicon can be doped with phosphorous by flowing phosphene (PH_3) in the CVD furnace during polysilicon deposition.

[0034] Next, in Fig. 5c, a dielectric layer 34 is deposited on top of the conductive layer 32. Preferably, the dielectric layer 34 is deposited using LPCVD. Preferably, the conductive layer 32 and the dielectric layer 34 are deposited in the same LPCVD step. During deposition, gas flow is changed from silane/phosphene (for doped polySi) to silane/ammonia for a silicon nitride dielectric. Alternatively, the gas flow can be changed relatively slowly so that a compositional transition region is formed between the conductive layer 32 and dielectric layer 34. In this case, the transition region will have an intermediate composition between dielectric and conductor.

[0035] Next, in Fig. 5d, photoresist (not shown) is deposited and patterned, and reactive ion etching is used to remove dielectric and conductive material from selected areas. This step exposes the PSG 30.

[0036] Finally, in Fig. 5e, the PSG 30 is removed in a release step. This can be performed in a fluorine-containing plasma, or using wet-etching techniques. A freestanding, released cantilever is provided after the release step.

[0037] Fig. 6 shows an alternative embodiment of the present invention where the conductive layer 26 is disposed within the dielectric layer (dividing it into two 'sublayers' 24a, 24b). This structure can be easily made by first depositing dielectric, followed by conductive material, and then more dielectric. All the layers can be deposited in the same LPCVD step by adjusting gas composition. In this embodiment,

the aggregate thickness of the two sublayers 24a, 24b should be at least 5 times the thickness of the conductive layer. More preferably, the aggregate thickness of the dielectric sublayers 24a, 24b are 10, 20, 50, or 100 times as thick as the conductive layer 26. Also preferably, the sublayers 24a, 24b have approximately equal thickness. Also, multiple conductive layers may be disposed within the dielectric layer.

[0038] Fig. 7 shows yet another embodiment of the present invention having top and bottom conductive layers 26a, 26b that are electrically coupled by via holes 40 through the dielectric layer 24. The vias can be made by reactive ion etching through the dielectric 24 before the deposition of the top conductive layer 26b. Conductive material, such as polysilicon, within the via holes 40 provides electrical connection between the top and bottom surfaces.

[0039] Fig. 8 shows yet another embodiment of the present invention where a thin, conductive layer 42 is conformally deposited on a dielectric 44 after the dielectric layer is etched. The view of Fig. 8 is a cross-sectional view perpendicular to the length of the cantilever 20. In this embodiment, the conductive layer 42 covers the top surface and sidewalls of the dielectric 44.

[0040] Figs. 9a-9f illustrate a preferred method for making the cantilever shown in Fig. 8. First, in Fig. 9a, PSG is deposited and patterned on a substrate. Next, a dielectric layer 50 is deposited on the PSG using LPCVD. In Fig. 9c, the dielectric layer 50 is etched using reactive ion etching. Alternatively, vias are also etched in the dielectric layer during this step. Next, in Fig. 9d, a conductive layer 52 is conformally deposited using LPCVD. Next, in Fig. 9e, the conductive layer is etched from the PSG using resist patterning and then reactive ion etching or other etching techniques. Finally, in Fig. 9f, the PSG is removed, releasing the cantilever. In this embodiment, the conductive layer thickness should be less than 1/5 of a width of the dielectric.

[0041] Alternatively, a conductive layer is deposited before the dielectric layer 50 is deposited so that the cantilever 20 is completely enclosed by conductive polysilicon. Fig. 10 shows a cross sectional view of a cantilever completely enclosed by polysilicon.

[0042] Fig. 11 shows a particularly useful application of the present invention. A dielectric layer 60 and conductive layers 62a, 62b are suspended above a substrate 64 by PSG 66 or similar material. The dielectric layer and conductive layers comprise a

diaphragm 65. Conductive pad 68 is disposed below the diaphragm 65. The conductive pad can be a doped region of a silicon substrate, for example. Applying a voltage between the conductive layers 62a, 62b and the conductive pad moves the diaphragm up or down, changing a gap distance 70.

[0043] In a particularly useful application of the present invention, thicknesses of the dielectric layer 60 and conductive layers 62a-b are selected so that the diaphragm 65 has a 1/4 wavelength thickness for a certain optical wavelength. This allows the device to be used as an electrostatically controlled variable optical reflector. The gap distance 70 may be changed to modulate the transmission or reflection of light of a given wavelength. The conductive layers provide for rapid electrostatic charge dissipation so that the device can operate at high frequency. It is preferable for the diaphragm to have top and bottom conductive layers as shown, but the diaphragm can optionally have a single top or bottom conductive layer. Clearly, such conductive layers could be patterned along the structural material allowing, for example, optical properties and electrical properties to be separated.

[0044] It is noted that the boundary between the conductive layer and the dielectric layer may not be well-defined. This is particularly true in embodiments where gas composition is changed relatively slowly during CVD deposition. In this case, the boundary between the dielectric layer and conductive layer (for purposes of determining layer thicknesses) is defined as where the silicon/nitrogen ratio is ½.

[0045] It will be appreciated by those skilled in the art of surface micromachining that many other more complex structures can be made according to the present invention. For example, electrostatic motors, switches, comb drives and other devices comprising dielectric with an attached conductive layer can fall within the scope of the present invention. In such devices, the polysilicon can provide the conductivity necessary for operation.

[0046] It is also noted that the microstructures of the present invention are not necessarily released by wet etching PSG, or other release materials. Microstructures according to the present invention can be released by bulk micromachining (e.g. anisotropic wet etching, isotropic wet etching, or isotropic dry etching) of the substrate material.

[0047] These and other advantages of the present invention will be apparent to those skilled in the art from the foregoing specification. Accordingly, it will be recognized by those skilled in the art that changes or modifications may be made to the above-described embodiments without departing from the broad inventive concepts of the invention. It should therefore be understood that this invention is not limited to the particular embodiments described herein, but is intended to include all changes and modifications that are within the scope and spirit of the invention as set forth in the claims.